PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-186194
(43)Date of publication of application : 09.07.1999

(51)Int.Cl. H01L 21/285
C23C 14/34
H01L 21/203
H01L 29/78

(21)Application number : 09-351304
(22)Date of filing : 19.12.1997

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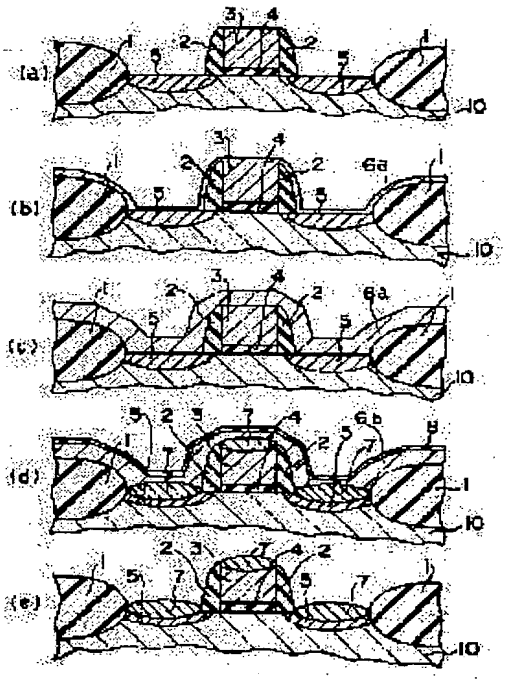
(54) FABRICATION OF SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a fabrication method of semiconductor device in which an isolation film is prevented from being broken by the secondary electrons of plasma in forming a metal film on an element fabricated on the surface of a semiconductor substrate.
SOLUTION: Ti 6a is deposited by sputtering on a semiconductor substrate 10 where an element is formed on the surface thereof. The Ti 6a is deposited using a general DC magnetron sputtering system under conditions of Ar gas pressure of 1 mTorr and DC power of 4.4 kW. Under that deposition conditions, the Ti layer 6a is continuous in the initial deposition stage of 1 sec after starting discharge and local charge up is prevented even if the Ti layer 6a is charged with secondary electrons generated by sputtering plasma. A Ti layer 6a of about 300 Å thick is formed on the entire surface by subsequent sputtering.



LEGAL STATUS

[Date of request for examination] 19.12.1997
[Date of sending the examiner's decision of rejection] 14.03.2001
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]
[Number of appeal against examiner's decision of rejection]
[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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CLAIMS

[Claim(s)]
[Claim 1] It is the manufacture approach of the semiconductor device characterized by being carried out on the conditions from which the metal membrane by which the formation process of said metal membrane continued even after [of membrane formation initiation] 1 second in the manufacture approach of a semiconductor device of having the process which forms a component on a silicon substrate, and the process which forms a metal membrane on said component is obtained.
[Claim 2] Said metal membrane is the manufacture approach of the semiconductor device according to claim 1 characterized by being formed of sputtering.
[Claim 3] Said conditions are the manufacture approach of the semiconductor device according to claim 2 characterized by setting direct current power when forming a metal membrane to 4 thru/or 10kW.
[Claim 4] Said metal membrane is the manufacture approach of the semiconductor device according to claim 1 characterized by being formed of plasma chemistry vapor growth.
[Claim 5] Said metal membrane is the manufacture approach of a semiconductor device given in claim 1 characterized by consisting of a metal which reacts with silicon and forms metal silicide thru/or any 1 term of 4.
[Claim 6] Said metal membrane is the manufacture approach of the semiconductor device according to claim 5 characterized by consisting of at least one sort of metals chosen from the group which consists of Ti, Co, nickel, Mo, W, and Ta.
[Claim 7] The process which forms a component on said silicon substrate is the manufacture approach of a semiconductor device given in claim 1 characterized by having the process which forms an insulator layer alternatively on said silicon substrate, the process which forms a gate electrode on said insulator layer, and the process which forms a diffusion layer in the front face of said silicon substrate thru/or any 1 term of 6.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] In the production process of a semiconductor device, this invention can prevent destruction of the insulator layer formed on the semi-conductor substrate, and relates to the manufacture approach of a semiconductor device that a reliable semiconductor device can be manufactured by the high yield by this.
[0002]
[Description of the Prior Art] Recently, detailed-ization of a component is advanced with detailed-izing of semiconductor integrated circuits, such as LSI. For example, while the impurity diffused layer used as a source-drain field is formed shallowly, low area is formed and wiring which connects between components is also formed into low width of face. Therefore, an impurity diffused layer and the electric resistance in wiring increase, and it has been the failure of improvement in the speed of component actuation. Then, in the conventional semiconductor device, by forming a refractory metal silicide layer on the surface of an impurity diffused layer, resistance is reduced and improvement in a component working speed is aimed at. The thing using Ti silicide layer is proposed as one example of a semiconductor device which aimed at improvement in a component working speed (USP4,855,798).
[0003] Drawing 5 (a) thru/or 5 (d) are the sectional views showing the manufacture approach of the conventional semiconductor device of having aimed at improvement in a working speed using Ti silicide layer, in order of a process. As shown in drawing 5 (a), the component demarcation membrane 11 which consists of an insulator layer is alternatively formed in the front face of the semi-conductor substrate 20, and this divides a component field. Next, on the front face of this component field, after carrying out sequential membrane formation of an oxide film (not shown) and the polish recon film (not shown), the gate electrode 13 which consists of the gate oxide 14 and the polish recon film which consist of an oxide film is formed by carrying out patterning of these to a gate configuration by the lithography method and the dry etching method. Then, the side-attachment-wall insulator layer 12 which becomes the side-attachment-wall section of the gate electrode 13 from the oxide film which remained is formed by forming an oxide film (not shown) all over these, and carrying out the etching back of this oxide film. Then, ion is poured in from these upper parts and a diffusion layer 15 is alternatively formed by heat-treating a substrate 20.
[0004] Then, the wet etching which used the fluoric acid which had the natural oxidation film (not shown) formed on the gate electrode 13 and the diffusion layer 15 diluted removes. Then, as shown in drawing 5 (b), Ti film 19b is formed by about 300A thickness on these front faces by sputtering.
[0005] Then, as shown in drawing 5 (c), Ti silicide layer 17 of 49 layers of C which consists of TiSi2 of high resistance is formed in the field to which the field where Ti film 19b and the gate electrode 13 touch, and Ti film 19b and a diffusion layer 15 touch in self align by heat-treating to a substrate. Since it has heat-treated under nitrogen-gas-atmosphere mind at this time, the TiN layer 18 of thickness with a divisor of 10A is formed in the front face of Ti film 19b.
[0006] Then, as shown in drawing 5 (d), unreacted Ti film 19c on the component demarcation

membrane 11 and the side-attachment-wall insulator layer 12 and the TiN layer 18 are removed. Then, Ti silicide layer 17 of high resistance is transferred to Ti silicide layer of 54 layers of C which consists of TiSi2 of low resistance by heat-treating under nitrogen-gas-atmosphere mind to a substrate. Thus, in the conventional semiconductor device, the front face of a diffusion layer 15 is formed into low resistance, and improvement in the working speed of a component is aimed at.

[0007] However, in manufacturing a semiconductor device by the manufacture approach shown in drawing 5 , there is a trouble shown below. That is, the secondary electron contained in the plasma etc. at the time of sputtering may run through gate oxide 14 from Ti film 19b, and may flow to a substrate 20. Thus, if a current flows between Ti film 19b and a substrate 20, the insulation of gate oxide 14 will be destroyed and it will result in a poor proof pressure. Thereby, while the dependability of a semiconductor device falls remarkably, the manufacture yield of a semiconductor device falls.

[0008] Then, the approach of forming Ti film using the usual not the sputtering method but collimation sputtering method is proposed as an approach of preventing destruction of the gate oxide 14 by electrification of a secondary electron. Drawing 6 is the mimetic diagram showing the usual sputtering method by DC magnetron, and drawing 7 is the mimetic diagram showing the collimation sputtering method. As shown in drawing 6 and drawing 7 , the target 31 is arranged in the sputtering system (not shown), and the cathode magnet 36 is arranged on the top face of this target 31. And on the stage 34 arranged under the target 31, after arranging a substrate 33, the plasma 32 is generated between a substrate 33 and a target 31, and Ti film is formed on a substrate 33. The membrane formation approach of this Ti film is the same, when using the usual sputtering approach and using the collimation sputtering method.

[0009] However, since the plasma 32 is generated by right above [of a substrate 33] when using the usual sputtering method as shown in drawing 6 , a secondary electron tends to jump into a substrate 33. On the other hand, in the collimation sputtering method shown in drawing 7 , the collimator 35 is arranged between a substrate 33 and the plasma 32. In case two or more holes which penetrate this collimator 35 in parallel with that direction of board thickness are prepared and the plasma 32 passes the hole of a collimator 35, the trap of the secondary electron from the plasma 32 is carried out to a collimator 35. Therefore, it can control that dielectric breakdown of gate oxide 14 shown in drawing 5 occurs.

[0010]

[Problem(s) to be Solved by the Invention] However, since Ti film adheres to a collimator 35 and the path of a collimator 35 contracts in using the collimation sputtering method shown in drawing 7 , amendment of a membrane formation rate is needed with consumption of a target, and there is a trouble that management is difficult. Moreover, since Ti film adheres to a collimator 35, the consumption effectiveness of a target falls and a manufacturing cost rises. These serve as a big trouble, when manufacturing a semiconductor device in large quantities. Originally, even if the collimation sputtering method is the case that the aspect ratio which shows the depth of the hole to the path of the hole formed in the substrate front face is large, it is an approach for forming the film in the state of good covering on the base of a hole. Therefore, in the formation process of Ti film with which high covering nature is not demanded, using the collimation sputtering method has few advantages, when an above-mentioned trouble is taken into consideration.

[0011] Thus, if the case where a semiconductor device is mass-produced is taken into consideration, even if it is desirable to form membranes by the usual sputtering method as for Ti film for forming Ti silicide film and it uses this approach, it is required that the manufacture approach of a semiconductor device which dielectric breakdown of gate dielectric film 14 does not generate should be established.

[0012] When this invention is made in view of this trouble and it forms a metal membrane on the component of a semi-conductor substrate front face, it aims at offering the manufacture approach of the semiconductor device which can control that the insulator layer of a component is destroyed by the secondary electron of the plasma.

[0013]

[Means for Solving the Problem] In the manufacture approach of a semiconductor device of having the process at which the manufacture approach of the semiconductor device concerning this invention forms a component on a silicon substrate, and the process which forms a metal membrane on said component, the formation process of said metal membrane is characterized by being carried out on the conditions from which the metal membrane which continued even after [of membrane formation initiation] 1 second is obtained.

[0014] As for this metal membrane, it is desirable to form membranes on the conditions which could form by sputtering and set direct current power to 4 thru/or 10kW in this case. Moreover, said metal membrane can also be formed by plasma chemistry vapor growth.

[0015] Furthermore, said metal membrane shall consist of at least one sort of metals chosen from the group which shall consist of a metal which reacts with silicon and forms metal silicide, for example, consists of Ti, Co, nickel, Mo, W, and Ta.

[0016] Furthermore, the process which forms a component on said silicon substrate can have the process which forms an insulator layer alternatively on said silicon substrate, the process which forms a gate electrode on said insulator layer, and the process which forms a diffusion layer in the front face of said silicon substrate again.

[0017] In addition, in this invention, the continuous film means [be / it / under / graph / which took the sheet resistance of a metal membrane to the Y-axis, and took sputtering time amount to the X-axis / setting] the case where the actual measurement of the sheet resistance by sputtering time amount is approximated by formula Y=a/X (a is a constant). However, this actual measurement does not need to be on the above-mentioned formula strictly, and an actual measurement should just be in less than **40% of range from the above-mentioned formula.

[0018] As a result of doing experiment research variously, when a metal membrane was formed on a component by the conventional manufacture approach that this invention person etc. should prevent destruction of the insulator layer by the secondary electron of the plasma, in the early stages of membrane formation, that a metal membrane adheres to a component front face as island-like discontinuity film found out that it was the cause of dielectric breakdown. That is, as shown in drawing 4 (a), after starting membrane formation of Ti film (metal membrane) 19a, in early stages of 2 thru/or the membrane formation for 3 seconds, Ti film 19a adheres to a component front face as discontinuity film of an island condition, and continuous Ti film is formed after that. Since discontinuous Ti film 19a in early stages of [this] membrane formation is in the condition of having floated electrically, the secondary electron contained in the plasma for sputtering etc. is charged in Ti film 19a, and the local charge up of high potential happens. Therefore, when charge-up potential is raised more than a certain threshold, it runs through the insulator layer 14 which exists under Ti film 19a, and a current flows to a substrate 20. Especially discontinuous Ti film 19a formed on the gate electrode 13 will run through gate oxide 14 through the gate electrode 13 which has floated electrically, and a current will flow to a substrate 20. Therefore, the insulation of gate oxide is destroyed and it results in a poor proof pressure.

[0019] Then, in this invention approach, the continuation film was obtained in early stages of membrane formation. That is, in this invention, as shown in drawing 4 (b), even after [of membrane formation initiation of Ti film] 1 second, it is the conditions in which continuous Ti film (metal membrane) 6a is formed, and Ti film is formed on a component. Therefore, since the local charge up does not occur even if the secondary electron generated by the plasma etc. is charged in Ti film 6a, it can prevent that gate oxide 4 is destroyed and, thereby, a reliable semiconductor device can be manufactured by the high yield.

[0020]

[Embodiment of the Invention] Hereafter, the semiconductor device concerning the example of this invention is concretely explained with reference to an attached drawing. Drawing 1 (a) thru/or 1 (d) are the sectional views showing the manufacture approach of the semiconductor device concerning the example of this invention in order of a process. As shown in drawing 1 (a), the component demarcation membrane 1 which consists of an insulator layer is alternatively formed in the front face of the semi-conductor substrate 10, and this divides a component field. Next, on the front face of this component field, after carrying out sequential membrane formation

of an oxide film (not shown) and the polish recon film (not shown), the gate electrode 3 which consists of the gate oxide 4 and the polish recon film which consist of an oxide film is formed by carrying out patterning of these to a gate configuration by the lithography method and the dry etching method. Then, the side-attachment-wall insulator layer 2 which becomes the side-attachment-wall section of the gate electrode 3 from the oxide film which remained is formed by forming an oxide film (not shown) all over these, and carrying out the etching back of this oxide film. Then, ion is poured in from these upper parts and a diffusion layer 5 is alternatively formed by heat-treating a substrate 10.

[0021] Then, the wet etching which used the fluoric acid which had the natural oxidation film (not shown) formed on the gate electrode 3 and the diffusion layer 5 diluted removes. Then, as shown in drawing 1 (b) and 1 (c), Ti film 6a is formed by the sputtering method on these front faces. In this example, Ti film 6a is formed using common DC magnetron sputtering system, the pressure of for example, Ar gas of membrane formation conditions is 1mTorr, and DC power (direct current power) is 4.4kW. Under these conditions, in the membrane formation early stages of after [of discharge starting] 1 second, as shown in drawing 1 (b), Ti film 6a is the continuation film, and even if the secondary electron generated by the plasma for sputtering etc. is charged, the local charge up is not started. Then, Ti film 6a of about 300A thickness is formed in the whole surface by carrying out sputtering succeedingly.

[0022] Then, as shown in drawing 1 (d), Ti silicide layer 7 of 49 layers of C which consists of TiSi2 of high resistance is formed in the field to which the field where the gate electrode 3 touches Ti film 6a, and Ti film 6a and a diffusion layer 5 touch in self align by using a lamp annealer and carrying out heat treatment for 30 seconds at 700 degrees C under nitrogen-gas-atmosphere mind. Since it has heat-treated under nitrogen-gas-atmosphere mind at this time, the TiN layer 8 of thickness with a divisor of 10A is formed in the front face of Ti film 6a.

[0023] Then, as shown in drawing 1 (e), the water solution of ammonia and hydrogen peroxide solution removes unreacted Ti film 6b on the component demarcation membrane 1 and the side-attachment-wall insulator layer 2, and the TiN layer 8. Then, Ti silicide layer 7 of high resistance is transferred to Ti silicide layer of 54 layers of C which consists of TiSi2 of low resistance by using a lamp annealer and carrying out heat treatment for 10 seconds at 850 degrees C under nitrogen-gas-atmosphere mind.

[0024] In this example, as shown in drawing 1 (b), in case Ti film 6a is formed by sputtering, also in the membrane formation early stages of after [of discharge starting] 1 second, an island condition will not be dotted by Ti film but it will turn into continuation film. Drawing 2 is the graphical representation showing the sheet resistance of the case where took sheet resistance along the axis of ordinate, took sputtering time amount along the axis of abscissa, and sputtering power is set to 4.4kW, and the case where sputtering power is set to 1.1kW, and the relation of sputtering time amount. In addition, in drawing 2 , the actual measurement of the sheet resistance by sputtering time amount when O sets sputtering power to 4.4kW is shown, and ** shows the measured value of the sheet resistance by the sputtering time amount at the time of setting sputtering power to 1.1kW. Moreover, in drawing 2 , since sputtering time amount is proportional to thickness, it can also be considered that an axis of abscissa is thickness. Generally, the sheet resistance and thickness of the continuation film have the relation shown in the following formula 1, and sheet resistance and thickness have the relation of an inverse proportion.

[0025]

[Equation 1] Sheet resistance = specific resistance / thickness, however specific resistance are fixed.

[0026] Fitting [with the least square method] using approximation function Y=a/X equivalent to the above-mentioned formula 1 as sputtering power is shown in the continuous line 21 in drawing in this example set to 4.4kW. That is, when sputtering power is set to 4.4kW, Ti film which continued 0.2 seconds after starting discharge is formed. On the other hand, if fitting is similarly carried out using approximation function Y=a/X when sputtering power is set to 1.1kW, as shown in the continuous line 22 in drawing, a surveying point and a fitting curve will shift greatly. This shows that a part of surveying point has not satisfied the above-mentioned formula 1.

[0027] Then, if fitting is carried out except for the surveying point of about 3 seconds after about the case where sputtering power is set to 1.1kW, using approximation function Y=a/(X-b) after starting discharge, as shown in the wavy line 23 in drawing, an approximation function and an actual measurement are in agreement like the case where sputtering power is set to 4.4kW. It is shown that the removed surveying point has not satisfied the above-mentioned formula by this. That is, when sputtering power is set to 1.1kW, after starting discharge, the continuation film is not formed in about 3 seconds, but being dotted with discontinuous Ti film of an island condition on a component is shown. In addition, if spacing of the adjacent film and the adjacent film is several angstroms thru/or several 10A even if it is the discontinuity film with which it is dotted, since a current will flow according to the tunneling effectiveness also on several V electrical potential difference, it can measure as sheet resistance. Then, in this invention, it is considered that the film with which it continued when the actual measurement of the sheet resistance by sputtering time amount was approximated by formula Y=a/X (a is a constant) was formed. However, this actual measurement shall not be on the above-mentioned formula strictly, and an actual measurement shall just be in less than **40% of range from the above-mentioned formula.

[0028] Drawing 3 is the graphical representation showing the defect incidence rate at the time of taking the defect incidence rate of gate pressure-proofing along an axis of ordinate, and forming Ti film by different sputtering power. In addition, the defect incidence rate was compared, when Ti film for forming Ti silicide layer on the example conditions (sputtering power: 4.4kW) in which the continuation film is formed even after [of membrane formation initiation] 1 second was formed, and when membranes were formed on the example conditions of a comparison (sputtering power: 1.1kW) that discontinuous Ti film of an island condition is formed in about 3 seconds after carrying out membrane formation initiation.

[0029] The measuring method of a defect incidence rate is explained below. First, after producing the test piece of the structure shown in drawing 1 (a) as a test pattern, the formation and removal of Ti film by sputtering are carried out on the front face, and the seal of approval of the electrical potential difference of 0 thru/or 12V is carried out in adjustable between a gate electrode and a substrate. At this time, the electrical potential difference on which dielectric breakdown of the gate oxide is carried out, and a high current flows is measured, and the case where this electrical potential difference is less than [3V] is judged as a defect. And the number of defects to the number of point of measurement is calculated as a percent defective. In addition, in the case of the normal gate oxide by which dielectric breakdown is not carried out, it depends also at the thickness and area, but thickness is about 100A, and if area is 2 about 32mm, the pressure resistance of about 10 V can be acquired, for example.

[0030] As shown in drawing 3 , when Ti film was formed having used sputtering power as 4.4kW, since it was the conditions in which Ti film which continued even after [of membrane formation initiation of Ti film] 1 second is formed, this condition had the very low proof-pressure percent defective of gate oxide, and became 0.58%. On the other hand, since the discontinuity film of an island condition is formed in about 3 seconds after starting discharge when Ti film is formed having used sputtering power as 1.1kW, a percent defective becomes 14.53% and the percent defective is increasing by about 25 times as compared with an example. Thus, on conditions in which the continuation film is formed even after [of membrane formation initiation] 1 second, if Ti film is formed by sputtering, the effectiveness which controls generating of the poor proof pressure of gate oxide can be acquired.

[0031] In addition, in the example shown in drawing 1 , although conditions in which the membrane formation rate of Ti film is raised and the continuation film is formed even after [of membrane formation initiation] 1 second by making DC power higher than the conventional range were set up, conditions other than DC power may be changed in this invention. For example, if it is the conditions which can form the metal membrane which continued even after [of membrane formation initiation] 1 second even if it optimizes other membrane formation parameters, such as gas pressure at the time of sputtering, or uses the approach of optimizing the cathode magnet for discharge, the same effectiveness as the case where sputtering power is set to 4.4kW can be acquired.

[0032] Moreover, in this invention, although the above-mentioned example showed the case where sputtering was used as the membrane formation approach of Ti film, even if it forms Ti film for example, on the conditions specified to this invention using a plasma-CVD method etc., the same effectiveness can be acquired. Furthermore, in the above-mentioned example, in order to form Ti silicide layer, the conditions at the time of membrane formation of Ti film were shown, but in this invention, for example like Co, nickel, Mo, W, and Ta, if it is the metal membrane which reacts with silicon and forms a silicide layer, the same effectiveness can be acquired.
[0033]
[Effect of the Invention] Since according to this invention the membrane formation conditions of the metal membrane formed on a component are specified appropriately and the continuation film is formed even after [of membrane formation initiation of a metal membrane] 1 second as explained in full detail above, destruction of the insulator layer generated when a metal membrane is charged can be prevented, and, thereby, a reliable semiconductor device can be manufactured by the high yield.

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TECHNICAL FIELD

[Field of the Invention] In the production process of a semiconductor device, this invention can prevent destruction of the insulator layer formed on the semi-conductor substrate, and relates to the manufacture approach of a semiconductor device that a reliable semiconductor device can be manufactured by the high yield by this.

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PRIOR ART

[Description of the Prior Art] Recently, detailed-ization of a component is advanced with detailed-izing of semiconductor integrated circuits, such as LSI. For example, while the impurity diffused layer used as a source-drain field is formed shallowly, low area is formed and wiring which connects between components is also formed into low width of face. Therefore, an impurity diffused layer and the electric resistance in wiring increase, and it has been the failure of improvement in the speed of component actuation. Then, in the conventional semiconductor device, by forming a refractory metal silicide layer on the surface of an impurity diffused layer, resistance is reduced and improvement in a component working speed is aimed at. The thing using Ti silicide layer is proposed as one example of a semiconductor device which aimed at improvement in a component working speed (USP4,855,798).
[0003] Drawing 5 (a) thru/or 5 (d) are the sectional views showing the manufacture approach of the conventional semiconductor device of having aimed at improvement in a working speed using Ti silicide layer, in order of a process. As shown in drawing 5 (a), the component demarcation membrane 11 which consists of an insulator layer is alternatively formed in the front face of the semi-conductor substrate 20, and this divides a component field. Next, on the front face of this component field, after carrying out sequential membrane formation of an oxide film (not shown) and the polish recon film (not shown), the gate electrode 13 which consists of the gate oxide 14 and the polish recon film which consist of an oxide film is formed by carrying out patterning of these to a gate configuration by the lithography method and the dry etching method. Then, the side-attachment-wall insulator layer 12 which becomes the side-attachment-wall section of the gate electrode 13 from the oxide film which remained is formed by forming an oxide film (not shown) all over these, and carrying out the etching back of this oxide film. Then, ion is poured in from these upper parts and a diffusion layer 15 is alternatively formed by heat-treating a substrate 20.
[0004] Then, the wet etching which used the fluoric acid which had the natural oxidation film (not shown) formed on the gate electrode 13 and the diffusion layer 15 diluted removes. Then, as shown in drawing 5 (b), Ti film 19b is formed by about 300A thickness on these front faces by sputtering.
[0005] Then, as shown in drawing 5 (c), Ti silicide layer 17 of 49 layers of C which consists of TiSi2 of high resistance is formed in the field to which the field where Ti film 19b and the gate electrode 13 touch, and Ti film 19b and a diffusion layer 15 touch in self align by heat-treating to a substrate. Since it has heat-treated under nitrogen-gas-atmosphere mind at this time, the TiN layer 18 of thickness with a divisor of 10A is formed in the front face of Ti film 19b.
[0006] Then, as shown in drawing 5 (d), unreacted Ti film 19c on the component demarcation membrane 11 and the side-attachment-wall insulator layer 12 and the TiN layer 18 are removed. Then, Ti silicide layer 17 of high resistance is transferred to Ti silicide layer of 54 layers of C which consists of TiSi2 of low resistance by heat-treating under nitrogen-gas-atmosphere mind to a substrate. Thus, in the conventional semiconductor device, the front face of a diffusion layer 15 is formed into low resistance, and improvement in the working speed of a component is aimed at.
[0007] However, in manufacturing a semiconductor device by the manufacture approach shown

in drawing 5 , there is a trouble shown below. That is, the secondary electron contained in the plasma etc. at the time of sputtering may run through gate oxide 14 from Ti film 19b, and may flow to a substrate 20. Thus, if a current flows between Ti film 19b and a substrate 20, the insulation of gate oxide 14 will be destroyed and it will result in a poor proof pressure. Thereby, while the dependability of a semiconductor device falls remarkably, the manufacture yield of a semiconductor device falls.

[0008] Then, the approach of forming Ti film using the usual not the sputtering method but collimation sputtering method is proposed as an approach of preventing destruction of the gate oxide 14 by electrification of a secondary electron. Drawing 6 is the mimetic diagram showing the usual sputtering method by DC magnetron, and drawing 7 is the mimetic diagram showing the collimation sputtering method. As shown in drawing 6 and drawing 7 , the target 31 is arranged in the sputtering system (not shown), and the cathode magnet 36 is arranged on the top face of this target 31. And on the stage 34 arranged under the target 31, after arranging a substrate 33, the plasma 32 is generated between a substrate 33 and a target 31, and Ti film is formed on a substrate 33. The membrane formation approach of this Ti film is the same, when using the usual sputtering approach and using the collimation sputtering method.

[0009] However, since the plasma 32 is generated by right above [of a substrate 33] when using the usual sputtering method as shown in drawing 6 , a secondary electron tends to jump into a substrate 33. On the other hand, in the collimation sputtering method shown in drawing 7 , the collimator 35 is arranged between a substrate 33 and the plasma 32. In case two or more holes which penetrate this collimator 35 in parallel with that direction of board thickness are prepared and the plasma 32 passes the hole of a collimator 35, the trap of the secondary electron from the plasma 32 is carried out to a collimator 35. Therefore, it can control that dielectric breakdown of gate oxide 14 shown in drawing 5 occurs.

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EFFECT OF THE INVENTION

[Effect of the Invention] Since according to this invention the membrane formation conditions of the metal membrane formed on a component are specified appropriately and the continuation film is formed even after [of membrane formation initiation of a metal membrane] 1 second as explained in full detail above, destruction of the insulator layer generated when a metal membrane is charged can be prevented, and, thereby, a reliable semiconductor device can be manufactured by the high yield.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, since Ti film adheres to a collimator 35 and the path of a collimator 35 contracts in using the collimation sputtering method shown in drawing 7 , amendment of a membrane formation rate is needed with consumption of a target, and there is a trouble that management is difficult. Moreover, since Ti film adheres to a collimator 35, the consumption effectiveness of a target falls and a manufacturing cost rises. These serve as a big trouble, when manufacturing a semiconductor device in large quantities. Originally, even if the collimation sputtering method is the case that the aspect ratio which shows the depth of the hole to the path of the hole formed in the substrate front face is large, it is an approach for forming the film in the state of good covering on the base of a hole. Therefore, in the formation process of Ti film with which high covering nature is not demanded, using the collimation sputtering method has few advantages, when an above-mentioned trouble is taken into consideration.
[0011] Thus, if the case where a semiconductor device is mass-produced is taken into consideration, even if it is desirable to form membranes by the usual sputtering method as for Ti film for forming Ti silicide film and it uses this approach, it is required that the manufacture approach of a semiconductor device which dielectric breakdown of gate dielectric film 14 does not generate should be established.
[0012] When this invention is made in view of this trouble and it forms a metal membrane on the component of a semi-conductor substrate front face, it aims at offering the manufacture approach of the semiconductor device which can control that the insulator layer of a component is destroyed by the secondary electron of the plasma.

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MEANS

[Means for Solving the Problem] In the manufacture approach of a semiconductor device of having the process at which the manufacture approach of the semiconductor device concerning this invention forms a component on a silicon substrate, and the process which forms a metal membrane on said component, the formation process of said metal membrane is characterized by being carried out on the conditions from which the metal membrane which continued even after [of membrane formation initiation] 1 second is obtained.
[0014] As for this metal membrane, it is desirable to form membranes on the conditions which could form by sputtering and set direct current power to 4 thru/or 10kW in this case. Moreover, said metal membrane can also be formed by plasma chemistry vapor growth.
[0015] Furthermore, said metal membrane shall consist of at least one sort of metals chosen from the group which shall consist of a metal which reacts with silicon and forms metal silicide, for example, consists of Ti, Co, nickel, Mo, W, and Ta.
[0016] Furthermore, the process which forms a component on said silicon substrate can have the process which forms an insulator layer alternatively on said silicon substrate, the process which forms a gate electrode on said insulator layer, and the process which forms a diffusion layer in the front face of said silicon substrate again.
[0017] In addition, in this invention, the continuous film means [be / it / under / graph / which took the sheet resistance of a metal membrane to the Y-axis, and took sputtering time amount to the X-axis / setting] the case where the actual measurement of the sheet resistance by sputtering time amount is approximated by formula Y=a/X (a is a constant). However, this actual measurement does not need to be on the above-mentioned formula strictly, and an actual measurement should just be in less than **40% of range from the above-mentioned formula.
[0018] As a result of doing experiment research variously, when a metal membrane was formed on a component by the conventional manufacture approach that this invention person etc. should prevent destruction of the insulator layer by the secondary electron of the plasma, in the early stages of membrane formation, that a metal membrane adheres to a component front face as island-like discontinuity film found out that it was the cause of dielectric breakdown. That is, as shown in drawing 4 (a), after starting membrane formation of Ti film (metal membrane) 19a, in early stages of 2 thru/or the membrane formation for 3 seconds, Ti film 19a adheres to a component front face as discontinuity film of an island condition, and continuous Ti film is formed after that. Since discontinuous Ti film 19a in early stages of [this] membrane formation is in the condition of having floated electrically, the secondary electron contained in the plasma for sputtering etc. is charged in Ti film 19a, and the local charge up of high potential happens. Therefore, when charge-up potential is raised more than a certain threshold, it runs through the insulator layer 14 which exists under Ti film 19a, and a current flows to a substrate 20. Especially discontinuous Ti film 19a formed on the gate electrode 13 will run through gate oxide 14 through the gate electrode 13 which has floated electrically, and a current will flow to a substrate 20. Therefore, the insulation of gate oxide is destroyed and it results in a poor proof pressure.
[0019] Then, in this invention approach, the continuation film was obtained in early stages of membrane formation. That is, in this invention, as shown in drawing 4 (b), even after [of

membrane formation initiation of Ti film] 1 second, it is the conditions in which continuous Ti film (metal membrane) 6a is formed, and Ti film is formed on a component. Therefore, since the local charge up does not occur even if the secondary electron generated by the plasma etc. is charged in Ti film 6a, it can prevent that gate oxide 4 is destroyed and, thereby, a reliable semiconductor device can be manufactured by the high yield.

[0020]

[Embodiment of the Invention] Hereafter, the semiconductor device concerning the example of this invention is concretely explained with reference to an attached drawing. Drawing 1 (a) thru/or 1 (d) are the sectional views showing the manufacture approach of the semiconductor device concerning the example of this invention in order of a process. As shown in drawing 1 (a), the component demarcation membrane 1 which consists of an insulator layer is alternatively formed in the front face of the semi-conductor substrate 10, and this divides a component field. Next, on the front face of this component field, after carrying out sequential membrane formation of an oxide film (not shown) and the polish recon film (not shown), the gate electrode 3 which consists of the gate oxide 4 and the polish recon film which consist of an oxide film is formed by carrying out patterning of these to a gate configuration by the lithography method and the dry etching method. Then, the side-attachment-wall insulator layer 2 which becomes the side-attachment-wall section of the gate electrode 3 from the oxide film which remained is formed by forming an oxide film (not shown) all over these, and carrying out the etching back of this oxide film. Then, ion is poured in from these upper parts and a diffusion layer 5 is alternatively formed by heat-treating a substrate 10.

[0021] Then, the wet etching which used the fluoric acid which had the natural oxidation film (not shown) formed on the gate electrode 3 and the diffusion layer 5 diluted removes. Then, as shown in drawing 1 (b) and 1 (c), Ti film 6a is formed by the sputtering method on these front faces. In this example, Ti film 6a is formed using common DC magnetron sputtering system, the pressure of for example, Ar gas of membrane formation conditions is 1mTorr, and DC power (direct current power) is 4.4kW. Under these conditions, in the membrane formation early stages of after [of discharge starting] 1 second, as shown in drawing 1 (b), Ti film 6a is the continuation film, and even if the secondary electron generated by the plasma for sputtering etc. is charged, the local charge up is not started. Then, Ti film 6a of about 300A thickness is formed in the whole surface by carrying out sputtering succeedingly.

[0022] Then, as shown in drawing 1 (d), Ti silicide layer 7 of 49 layers of C which consists of TiSi2 of high resistance is formed in the field to which the field where the gate electrode 3 touches Ti film 6a, and Ti film 6a and a diffusion layer 5 touch in self align by using a lamp annealer and carrying out heat treatment for 30 seconds at 700 degrees C under nitrogen-gas-atmosphere mind. Since it has heat-treated under nitrogen-gas-atmosphere mind at this time, the TiN layer 8 of thickness with a divisor of 10A is formed in the front face of Ti film 6a.

[0023] Then, as shown in drawing 1 (e), the water solution of ammonia and hydrogen peroxide solution removes unreacted Ti film 6b on the component demarcation membrane 1 and the side-attachment-wall insulator layer 2, and the TiN layer 8. Then, Ti silicide layer 7 of high resistance is transferred to Ti silicide layer of 54 layers of C which consists of TiSi2 of low resistance by using a lamp annealer and carrying out heat treatment for 10 seconds at 850 degrees C under nitrogen-gas-atmosphere mind.

[0024] In this example, as shown in drawing 1 (b), in case Ti film 6a is formed by sputtering, also in the membrane formation early stages of after [of discharge starting] 1 second, an island condition will not be dotted by Ti film but it will turn into continuation film. Drawing 2 is the graphical representation showing the sheet resistance of the case where took sheet resistance along the axis of ordinate, took sputtering time amount along the axis of abscissa, and sputtering power is set to 4.4kW, and the case where sputtering power is set to 1.1kW, and the relation of sputtering time amount. In addition, in drawing 2 , the actual measurement of the sheet resistance by sputtering time amount when O sets sputtering power to 4.4kW is shown, and ** shows the measured value of the sheet resistance by the sputtering time amount at the time of setting sputtering power to 1.1kW. Moreover, in drawing 2 , since sputtering time amount is proportional to thickness, it can also be considered that an axis of abscissa is thickness.

Generally, the sheet resistance and thickness of the continuation film have the relation shown in the following formula 1, and sheet resistance and thickness have the relation of an inverse proportion.

[0025]

[Equation 1] Sheet resistance = specific resistance / thickness, however specific resistance are fixed.

[0026] Fitting [with the least square method] using approximation function Y=a/X equivalent to the above-mentioned formula 1 as sputtering power is shown in the continuous line 21 in drawing in this example set to 4.4kW. That is, when sputtering power is set to 4.4kW, Ti film which continued 0.2 seconds after starting discharge is formed. On the other hand, if fitting is similarly carried out using approximation function Y=a/X when sputtering power is set to 1.1kW, as shown in the continuous line 22 in drawing, a surveying point and a fitting curve will shift greatly. This shows that a part of surveying point has not satisfied the above-mentioned formula 1.

[0027] Then, if fitting is carried out except for the surveying point of about 3 seconds after about the case where sputtering power is set to 1.1kW, using approximation function Y=a/(X-b) after starting discharge, as shown in the wavy line 23 in drawing, an approximation function and an actual measurement are in agreement like the case where sputtering power is set to 4.4kW. It is shown that the removed surveying point has not satisfied the above-mentioned formula by this. That is, when sputtering power is set to 1.1kW, after starting discharge, the continuation film is not formed in about 3 seconds, but being dotted with discontinuous Ti film of an island condition on a component is shown. In addition, if spacing of the adjacent film and the adjacent film is several angstroms thru/or several 10A even if it is the discontinuity film with which it is dotted, since a current will flow according to the tunneling effectiveness also on several V electrical potential difference, it can measure as sheet resistance. Then, in this invention, it is considered that the film with which it continued when the actual measurement of the sheet resistance by sputtering time amount was approximated by formula Y=a/X (a is a constant) was formed. However, this actual measurement shall not be on the above-mentioned formula strictly, and an actual measurement shall just be in less than **40% of range from the above-mentioned formula.

[0028] Drawing 3 is the graphical representation showing the defect incidence rate at the time of taking the defect incidence rate of gate pressure-proofing along an axis of ordinate, and forming Ti film by different sputtering power. In addition, the defect incidence rate was compared, when Ti film for forming Ti silicide layer on the example conditions (sputtering power: 4.4kW) in which the continuation film is formed even after [of membrane formation initiation] 1 second was formed, and when membranes were formed on the example conditions of a comparison (sputtering power: 1.1kW) that discontinuous Ti film of an island condition is formed in about 3 seconds after carrying out membrane formation initiation.

[0029] The measuring method of a defect incidence rate is explained below. First, after producing the test piece of the structure shown in drawing 1 (a) as a test pattern, the formation and removal of Ti film by sputtering are carried out on the front face, and the seal of approval of the electrical potential difference of 0 thru/or 12V is carried out in adjustable between a gate electrode and a substrate. At this time, the electrical potential difference on which dielectric breakdown of the gate oxide is carried out, and a high current flows is measured, and the case where this electrical potential difference is less than [3V] is judged as a defect. And the number of defects to the number of point of measurement is calculated as a percent defective. In addition, in the case of the normal gate oxide by which dielectric breakdown is not carried out, it depends also at the thickness and area, but thickness is about 100A, and if area is 2 about 32mm, the pressure resistance of about 10 V can be acquired, for example.

[0030] As shown in drawing 3 , when Ti film was formed having used sputtering power as 4.4kW, since it was the conditions in which Ti film which continued even after [of membrane formation initiation of Ti film] 1 second is formed, this condition had the very low proof-pressure percent defective of gate oxide, and became 0.58%. On the other hand, since the discontinuity film of an island condition is formed in about 3 seconds after starting discharge when Ti film is formed having used sputtering power as 1.1kW, a percent defective becomes 14.53% and the percent

defective is increasing by about 25 times as compared with an example. Thus, on conditions in which the continuation film is formed even after [of membrane formation initiation] 1 second, if Ti film is formed by sputtering, the effectiveness which controls generating of the poor proof pressure of gate oxide can be acquired.

[0031] In addition, in the example shown in drawing 1 , although conditions in which the membrane formation rate of Ti film is raised and the continuation film is formed even after [of membrane formation initiation] 1 second by making DC power higher than the conventional range were set up, conditions other than DC power may be changed in this invention. For example, if it is the conditions which can form the metal membrane which continued even after [of membrane formation initiation] 1 second even if it optimizes other membrane formation parameters, such as gas pressure at the time of sputtering, or uses the approach of optimizing the cathode magnet for discharge, the same effectiveness as the case where sputtering power is set to 4.4kW can be acquired.

[0032] Moreover, in this invention, although the above-mentioned example showed the case where sputtering was used as the membrane formation approach of Ti film, even if it forms Ti film for example, on the conditions specified to this invention using a plasma-CVD method etc., the same effectiveness can be acquired. Furthermore, in the above-mentioned example, in order to form Ti silicide layer, the conditions at the time of membrane formation of Ti film were shown, but in this invention, for example like Co, nickel, Mo, W, and Ta, if it is the metal membrane which reacts with silicon and forms a silicide layer, the same effectiveness can be acquired.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (a) Or 1 (d) is the sectional view showing the manufacture approach of the semiconductor device concerning the example of this invention in order of a process.
[Drawing 2] It is the graphical representation showing the sheet resistance of the case where took sheet resistance along the axis of ordinate, took sputtering time amount along the axis of abscissa, and sputtering power is set to 4.4kW, and the case where sputtering power is set to 1.1kW, and the relation of sputtering time amount.
[Drawing 3] It is the graphical representation showing the defect incidence rate at the time of taking the defect incidence rate of gate pressure-proofing along an axis of ordinate, and forming Ti film by different sputtering power.
[Drawing 4] (a) is the sectional view showing the initial state of the metal membrane at the time of forming a metal membrane on a component using the conventional manufacture approach, and drawing 4 (b) is the sectional view showing the initial state of the metal membrane at the time of forming a metal membrane on a component using the manufacture approach concerning this invention.
[Drawing 5] (a) Or 5 (d) is the sectional view showing the manufacture approach of the conventional semiconductor device of having aimed at improvement in a working speed using Ti silicide layer, in order of a process.
[Drawing 6] It is the mimetic diagram showing the usual sputtering method by DC magnetron.
[Drawing 7] It is the mimetic diagram showing the collimation sputtering method.
[Description of Notations]
1 11; component demarcation membrane
2 12; side-attachment-wall insulator layer
3 13; gate electrode
4 14; gate oxide
5 15; diffusion layer
6a, 6b, 19a, 19b, 19 c;Ti film
7 and 17;Ti silicide layer
8 and 18;TiN layer
10 20; semi-conductor substrate
31; target
32; plasma
33; substrate
34; stage
35; collimator
36; cathode magnet

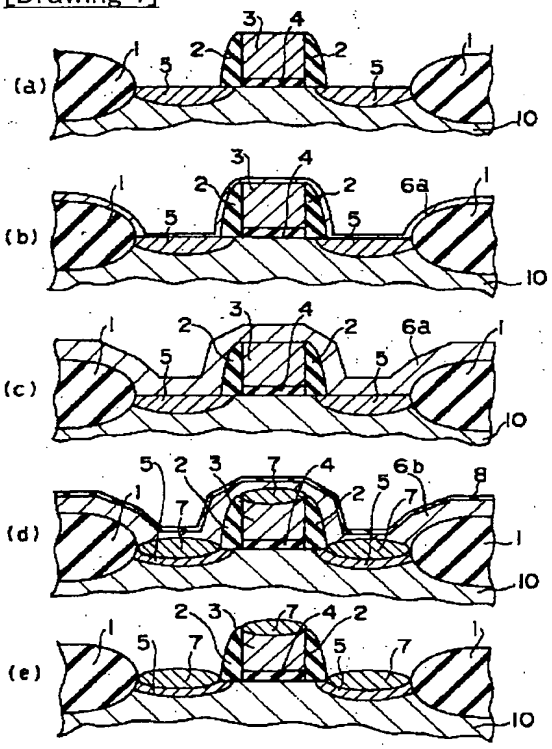
[Translation done.]

* NOTICES *

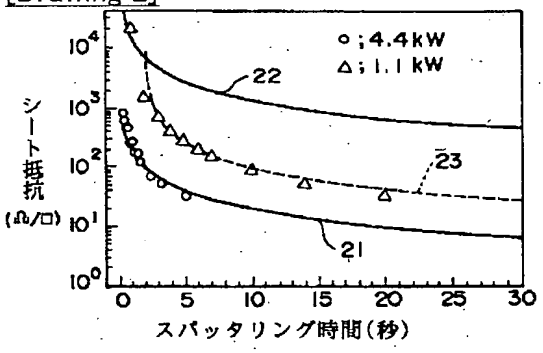
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

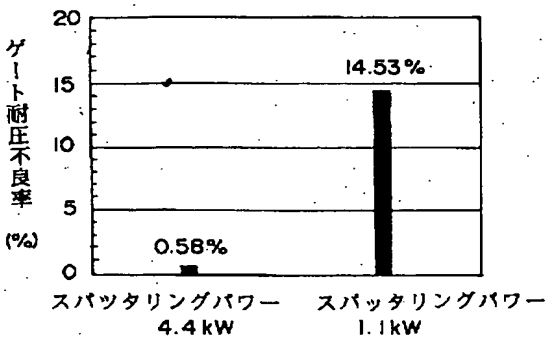
[Drawing 1]



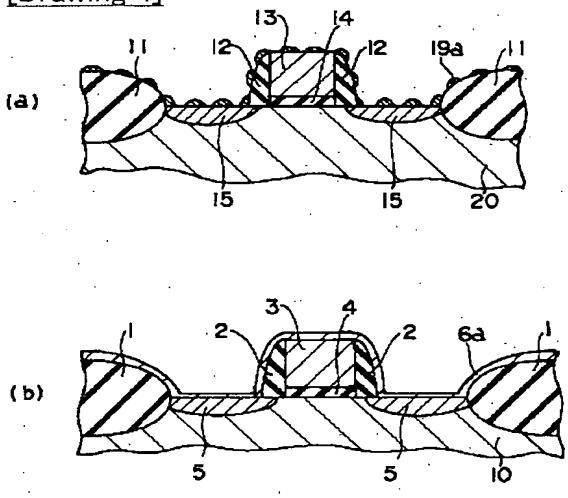
[Drawing 2]



[Drawing 3]

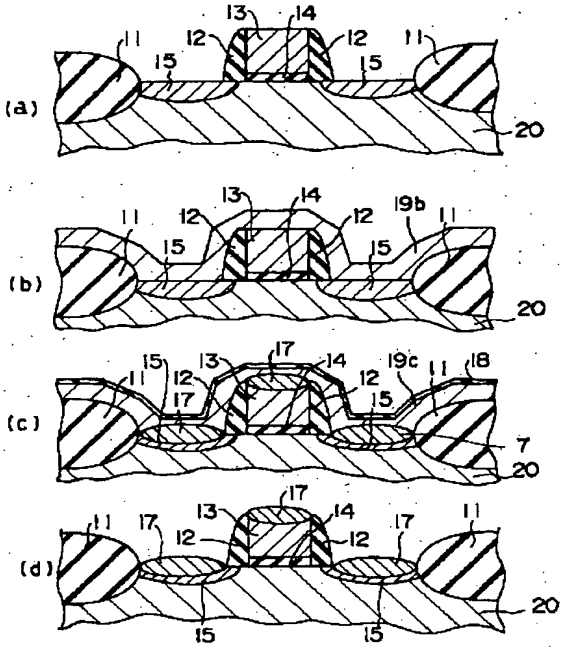


[Drawing 4]



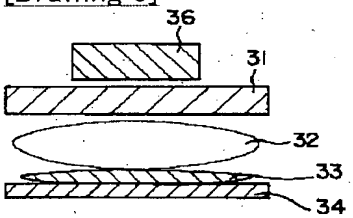
1,11；素子分離膜　5,15；拡散層
2,12；側壁絶縁膜　6a,19a；Ti膜
3,13；ゲート電極　10,20；半導体基板
4,14；ゲート酸化膜

[Drawing 5]

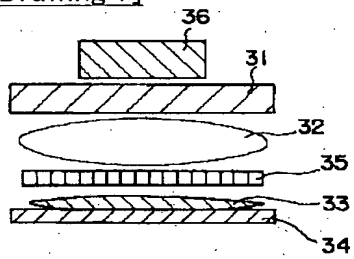


１１；素子分離膜　　１７；Ｔｉシリサイド層
１２；側壁絶縁膜　　１８；ＴｉＮ層
１３；ゲート電極　　１９ｂ,１９ｃ；Ｔｉ膜
１４；ゲート酸化膜　　２０；半導体基板
１５；拡散層

[Drawing 6]



[Drawing 7]



３１；ターゲット　　３４；ステージ
３２；プラズマ　　３５；コリメータ
３３；基板　　３６；カソードマグネット

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平11－186194

(43)公開日　平成11年(1999)７月９日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｈ０１Ｌ　21/285		Ｈ０１Ｌ　21/285	Ｓ
Ｃ２３Ｃ　14/34		Ｃ２３Ｃ　14/34	Ｒ
Ｈ０１Ｌ　21/203		Ｈ０１Ｌ　21/203	Ｓ
29/78		29/78	３０１Ｇ

審査請求　有　　請求項の数７　ＯＬ　（全７頁）

(21)出願番号　特願平9－351304

(22)出願日　平成９年(1997)12月19日

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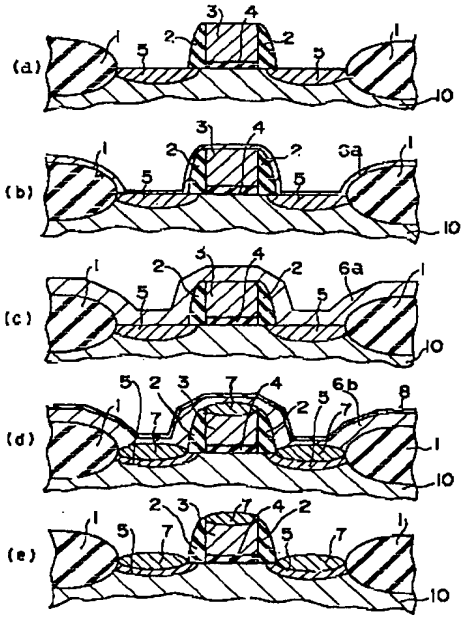
(54)【発明の名称】　半導体装置の製造方法

(57)【要約】

【課題】　半導体基板表面の素子上に金属膜を形成する場合に、プラズマの２次電子によって素子の絶縁膜が破壊されることを抑制することができる半導体装置の製造方法を提供する。

【解決手段】　表面に素子が形成された半導体基板１０の上にＴｉ膜６ａをスパッタリング法により形成する。このＴｉ膜６ａは、一般的なＤＣマグネトロンスパッタリング装置を使用して成膜し、成膜条件は、Ａｒガスの圧力が１ｍＴｏｒｒであり、直流電力は４．４ｋＷである。この条件下では、放電開始から１秒後までの成膜初期においても、Ｔｉ膜６ａが連続膜となっており、スパッタリング用のプラズマ等により発生する２次電子が帯電しても、局所的なチャージアップを起こすことがない。その後、引き続いてスパッタリングすることにより、約３００Åの膜厚のＴｉ膜６ａを全面に形成する。



【特許請求の範囲】
【請求項１】　シリコン基板上に素子を形成する工程と、前記素子上に金属膜を形成する工程と、を有する半導体装置の製造方法において、前記金属膜の形成工程は、成膜開始から１秒後までに連続した金属膜が得られる条件で行われることを特徴とする半導体装置の製造方法。
【請求項２】　前記金属膜はスパッタリングにより形成されることを特徴とする請求項１に記載の半導体装置の製造方法。
【請求項３】　前記条件は、金属膜を成膜するときの直流電力を４乃至１０ｋＷとしたものであることを特徴とする請求項２に記載の半導体装置の製造方法。
【請求項４】　前記金属膜はプラズマ化学気相成長法により形成されることを特徴とする請求項１に記載の半導体装置の製造方法。
【請求項５】　前記金属膜は、シリコンと反応して金属シリサイドを形成する金属からなることを特徴とする請求項１乃至４のいずれか１項に記載の半導体装置の製造方法。
【請求項６】　前記金属膜は、Ｔｉ、Ｃｏ、Ｎｉ、Ｍｏ、Ｗ及びＴａからなる群から選択された少なくとも１種の金属からなることを特徴とする請求項５に記載の半導体装置の製造方法。
【請求項７】　前記シリコン基板上に素子を形成する工程は、前記シリコン基板上に絶縁膜を選択的に形成する工程と、前記絶縁膜上にゲート電極を形成する工程と、前記シリコン基板の表面に拡散層を形成する工程と、を有することを特徴とする請求項１乃至６のいずれか１項に記載の半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は半導体装置の製造工程において、半導体基板上に形成された絶縁膜の破壊を防止することができ、これにより、信頼性が高い半導体装置を高歩留まりで製造することができる半導体装置の製造方法に関する。
【０００２】
【従来の技術】近時、ＬＳＩ等の半導体集積回路の微細化に伴って、素子の微細化が進められている。例えば、ソース－ドレイン領域となる不純物拡散層が浅く形成されると共に、低面積化されており、素子間を接続する配線も低幅化されている。従って、不純物拡散層及び配線における電気抵抗が増大し、素子動作の高速化の障害となっている。そこで、従来の半導体装置においては、不純物拡散層の表面に高融点金属シリサイド層を形成することにより抵抗を低下させて、素子動作速度の向上を図っている。素子動作速度の向上を図った半導体装置の１例として、Ｔｉシリサイド層を利用したものが提案されている（ＵＳＰ４，８５５，７９８）。
【０００３】図５（ａ）乃至５（ｄ）はＴｉシリサイド層を利用して動作速度の向上を図った従来の半導体装置の製造方法を工程順に示す断面図である。図５（ａ）に示すように、半導体基板２０の表面に絶縁膜からなる素子分離膜１１を選択的に形成し、これにより、素子領域を区画する。次に、この素子領域の表面上に、酸化膜（図示せず）及びポリシリコン膜（図示せず）を順次成膜した後、これらをリソグラフィ法及びドライエッチング法によりゲート形状にパターニングすることにより、酸化膜からなるゲート酸化膜１４及びポリシリコン膜からなるゲート電極１３を形成する。その後、これらの全面に酸化膜（図示せず）を形成し、この酸化膜をエッチングバックすることにより、ゲート電極１３の側壁部に、残存した酸化膜からなる側壁絶縁膜１２を形成する。その後、これらの上方からイオンを注入し、基板２０を熱処理することにより、拡散層１５を選択的に形成する。
【０００４】その後、ゲート電極１３及び拡散層１５上に形成された自然酸化膜（図示せず）を希釈された弗酸等を使用したウェットエッチングにより除去する。その後、図５（ｂ）に示すように、スパッタリングにより、これらの表面上に約３００Åの膜厚でＴｉ膜１９ｂを形成する。
【０００５】その後、図５（ｃ）に示すように、基板に対して熱処理を実施することにより、Ｔｉ膜１９ｂとゲート電極１３とが接触している領域及びＴｉ膜１９ｂと拡散層１５とが接触している領域に、高抵抗のＴｉ$Ｓｉ_2$からなるＣ４９層のＴｉシリサイド層１７が自己整合的に形成される。このとき、窒素雰囲気下において熱処理しているので、Ｔｉ膜１９ｂの表面に約数１０Åの膜厚のＴｉＮ層１８が形成される。
【０００６】その後、図５（ｄ）に示すように、素子分離膜１１及び側壁絶縁膜１２上の未反応のＴｉ膜１９ｃ及びＴｉＮ層１８を除去する。その後、基板に対して、窒素雰囲気下において、熱処理を実施することにより、高抵抗のＴｉシリサイド層１７を低抵抗のＴｉ$Ｓｉ_2$からなるＣ５４層のＴｉシリサイド層に転移させる。このようにして、従来の半導体装置においては、拡散層１５の表面を低抵抗化して、素子の動作速度の向上を図っている。
【０００７】しかし、図５に示す製造方法により半導体装置を製造する場合には、以下に示す問題点がある。即ち、スパッタリング時において、プラズマ等に含まれる２次電子がＴｉ膜１９ｂからゲート酸化膜１４を突き抜けて、基板２０に流れることがある。このように、Ｔｉ膜１９ｂと基板２０との間で電流が流れると、ゲート酸化膜１４の絶縁性が破壊され、耐圧不良に至る。これにより、半導体装置の信頼性が著しく低下すると共に、半導体装置の製造歩留まりが低下する。
【０００８】そこで、２次電子の帯電によるゲート酸化

膜１４の破壊を防止する方法として、通常のスパッタリング法ではなく、コリメートスパッタリング法を使用してＴｉ膜を成膜する方法が提案されている。図６はＤＣマグネトロンによる通常のスパッタリング法を示す模式図であり、図７はコリメートスパッタリング法を示す模式図である。図６及び図７に示すように、スパッタリング装置（図示せず）内にはターゲット３１が配置されており、このターゲット３１の上面にはカソードマグネット３６が配置されている。そして、ターゲット３１の下方に配置されたステージ３４上に、基板３３を配置した後、基板３３とターゲット３１との間にプラズマ３２を発生させて、基板３３上にＴｉ膜を形成する。このＴｉ膜の成膜方法は、通常のスパッタリング方法を使用する場合においても、コリメートスパッタリング法を使用する場合においても同様である。

【０００９】但し、図６に示すように、通常のスパッタリング法を使用する場合には、基板３３の直上にプラズマ３２が生成されるので、２次電子が基板３３に飛び込み易い。一方、図７に示すコリメートスパッタリング法においては、基板３３とプラズマ３２との間にコリメータ３５を配置している。このコリメータ３５は、その板厚方向に平行に貫通する複数個の孔が設けられているものであり、プラズマ３２がコリメータ３５の孔を通過する際に、プラズマ３２からの２次電子がコリメータ３５にトラップされる。従って、図５に示すゲート酸化膜１４の絶縁破壊が発生することを抑制することができる。

【００１０】

【発明が解決しようとする課題】しかしながら、図７に示すコリメートスパッタリング法を使用する場合には、コリメータ３５にＴｉ膜が付着して、コリメータ３５の径が縮小するので、ターゲットの消費に伴って成膜レートの補正が必要になり、管理が困難であるという問題点がある。また、コリメータ３５にＴｉ膜が付着するので、ターゲットの消費効率が低下し、製造コストが上昇する。これらは、半導体装置を大量に製造する場合に大きな問題点となる。本来、コリメートスパッタリング法は、基板表面に形成されたホールの径に対するホールの深さを示すアスペクト比が大きい場合であっても、ホールの底面上に、良好な被覆状態で膜を形成するための方法である。従って、高被覆性が要求されないＴｉ膜の形成工程において、コリメートスパッタリング法を使用することは、上述の問題点を考慮すると、利点が少ない。

【００１１】このように、半導体装置を量産する場合を考慮すると、Ｔｉシリサイド膜を形成するためのＴｉ膜は、通常のスパッタリング法により成膜することが望ましく、この方法を使用しても、ゲート絶縁膜１４の絶縁破壊が発生しないような半導体装置の製造方法を確立することが要求されている。

【００１２】本発明はかかる問題点に鑑みてなされたものであって、半導体基板表面の素子上に金属膜を形成する場合に、プラズマの２次電子によって素子の絶縁膜が破壊されることを抑制することができる半導体装置の製造方法を提供することを目的とする。

【００１３】

【課題を解決するための手段】本発明に係る半導体装置の製造方法は、シリコン基板上に素子を形成する工程と、前記素子上に金属膜を形成する工程と、を有する半導体装置の製造方法において、前記金属膜の形成工程は、成膜開始から１秒後までに連続した金属膜が得られる条件で行われることを特徴とする。

【００１４】この金属膜はスパッタリングにより形成することができ、この場合、直流電力を４乃至１０ｋＷとした条件で成膜することが好ましい。また、前記金属膜はプラズマ化学気相成長法により形成することもできる。

【００１５】更に、前記金属膜は、シリコンと反応して金属シリサイドを形成する金属からなるものとすることができ、例えば、Ｔｉ、Ｃｏ、Ｎｉ、Ｍｏ、Ｗ及びＴａからなる群から選択された少なくとも１種の金属からなるものとすることができる。

【００１６】更にまた、前記シリコン基板上に素子を形成する工程は、前記シリコン基板上に絶縁膜を選択的に形成する工程と、前記絶縁膜上にゲート電極を形成する工程と、前記シリコン基板の表面に拡散層を形成する工程と、を有することができる。

【００１７】なお、本発明において、連続した膜とは、Ｙ軸に金属膜のシート抵抗をとり、Ｘ軸にスパッタリング時間をとったグラフ中において、スパッタリング時間によるシート抵抗の実測値が、数式Ｙ＝ａ／Ｘ（ａは定数）で近似される場合をいう。但し、この実測値は厳密に上記数式上にある必要はなく、上記数式から±４０％以内の範囲に実測値があればよい。

【００１８】本発明者等がプラズマの２次電子による絶縁膜の破壊を防止すべく、種々実験研究した結果、従来の製造方法により素子上に金属膜を形成した場合は、成膜の初期において、金属膜が島状の不連続膜として素子表面に付着することが、絶縁破壊の原因であることを見い出した。即ち、図４（ａ）に示すように、Ｔｉ膜（金属膜）１９ａの成膜を開始してから２乃至３秒間の成膜初期では、Ｔｉ膜１９ａが島状態の不連続膜として素子表面に付着し、その後、連続的なＴｉ膜が形成される。この成膜初期の不連続なＴｉ膜１９ａは、電気的に浮いている状態であるので、スパッタリング用のプラズマ等に含まれる２次電子がＴｉ膜１９ａに帯電し、局所的な高電位のチャージアップが起こる。従って、あるしきい値以上にチャージアップ電位が高められた時に、Ｔｉ膜１９ａの下に存在する絶縁膜１４を突き抜けて、基板２０に電流が流れる。特に、ゲート電極１３上に形成された不連続なＴｉ膜１９ａは、電気的に浮いているゲート電極１３を介して、ゲート酸化膜１４を突き抜けて基板

２０へ電流が流れることになる。従って、ゲート酸化膜の絶縁性が破壊され、耐圧不良に至る。

【００１９】そこで、本発明方法においては、成膜の初期に連続膜が得られるようにした。即ち、本発明においては、図４（ｂ）に示すように、Ｔｉ膜の成膜開始から１秒後までに、連続したＴｉ膜（金属膜）６ａが形成される条件で、Ｔｉ膜を素子上に形成する。従って、プラズマ等により発生する２次電子がＴｉ膜６ａに帯電しても、局所的なチャージアップが発生しないので、ゲート酸化膜４が破壊されることを防止することができ、これにより、信頼性が高い半導体装置を高歩留まりで製造することができる。

【００２０】

【発明の実施の形態】以下、本発明の実施例に係る半導体装置について、添付の図面を参照して具体的に説明する。図１（ａ）乃至１（ｄ）は本発明の実施例に係る半導体装置の製造方法を工程順に示す断面図である。図１（ａ）に示すように、半導体基板１０の表面に絶縁膜からなる素子分離膜１を選択的に形成し、これにより、素子領域を区画する。次に、この素子領域の表面上に、酸化膜（図示せず）及びポリシリコン膜（図示せず）を順次成膜した後、これらをリソグラフィ法及びドライエッチング法によりゲート形状にパターニングすることにより、酸化膜からなるゲート酸化膜４及びポリシリコン膜からなるゲート電極３を形成する。その後、これらの全面に酸化膜（図示せず）を形成し、この酸化膜をエッチングバックすることにより、ゲート電極３の側壁部に、残存した酸化膜からなる側壁絶縁膜２を形成する。その後、これらの上方からイオンを注入し、基板１０を熱処理することにより、拡散層５を選択的に形成する。

【００２１】その後、ゲート電極３及び拡散層５上に形成された自然酸化膜（図示せず）を希釈された弗酸等を使用したウェットエッチングにより除去する。その後、図１（ｂ）及び１（ｃ）に示すように、これらの表面上にＴｉ膜６ａをスパッタリング法により形成する。本実施例においては、Ｔｉ膜６ａを一般的なＤＣマグネトロンスパッタリング装置を使用して成膜しており、成膜条件は、例えば、Ａｒガスの圧力が１ｍＴｏｒｒであり、ＤＣパワー（直流電力）は４．４ｋＷである。この条件下では、放電開始から１秒後までの成膜初期においても、図１（ｂ）に示すように、Ｔｉ膜６ａが連続膜となっており、スパッタリング用のプラズマ等により発生する２次電子が帯電しても、局所的なチャージアップを起こすことがない。その後、引き続いてスパッタリングすることにより、約３００Åの膜厚のＴｉ膜６ａを全面に形成する。

【００２２】その後、図１（ｄ）に示すように、ランプアニール装置を使用して、窒素雰囲気下において、７００℃で３０秒間の熱処理を実施することにより、Ｔｉ膜６ａとゲート電極３が接触している領域及びＴｉ膜６ａと拡散層５とが接触している領域に、高抵抗の$TiSi_2$からなるＣ４９層のＴｉシリサイド層７が自己整合的に形成される。このとき、窒素雰囲気下において熱処理しているので、Ｔｉ膜６ａの表面に約数１０Åの膜厚のＴｉＮ層８が形成される。

【００２３】その後、図１（ｅ）に示すように、素子分離膜１及び側壁絶縁膜２上の未反応のＴｉ膜６ｂ及びＴｉＮ層８をアンモニアと過酸化水素水との水溶液で除去する。その後、ランプアニール装置を使用して、窒素雰囲気下において、８５０℃で１０秒間の熱処理を実施することにより、高抵抗のＴｉシリサイド層７を低抵抗の$TiSi_2$からなるＣ５４層のＴｉシリサイド層に転移させる。

【００２４】本実施例においては、図１（ｂ）に示すように、スパッタリングによってＴｉ膜６ａを形成する際に、放電開始から１秒後までの成膜初期においても、Ｔｉ膜が島状態に点在した状態にならず、連続膜となる。図２は、縦軸にシート抵抗をとり、横軸にスパッタリング時間をとって、スパッタリングパワーを４．４ｋＷとした場合と、スパッタリングパワーを１．１ｋＷとした場合とのシート抵抗とスパッタリング時間の関係を示すグラフ図である。なお、図２において、○はスパッタリングパワーを４．４ｋＷとした場合のスパッタリング時間によるシート抵抗の実測値を示し、△はスパッタリングパワーを１．１ｋＷとした場合のスパッタリング時間によるシート抵抗の測定値を示す。また、図２において、スパッタリング時間は膜厚に比例しているので、横軸は膜厚とみなすこともできる。一般的に、連続膜のシート抵抗と膜厚とは下記数式１に示す関係にあり、シート抵抗と膜厚は反比例の関係にある。

【００２５】

【数１】シート抵抗＝比抵抗／膜厚

但し、比抵抗は一定である。

【００２６】スパッタリングパワーを４．４ｋＷとした本実施例においては、図中の実線２１に示すように、上記数式１に相当する近似関数Ｙ＝ａ／Ｘを使用して最小２乗法によってフィッティングすることができる。即ち、スパッタリングパワーを４．４ｋＷとしたときには、放電を開始してから０．２秒後においても、連続したＴｉ膜が形成される。一方、スパッタリングパワーを１．１ｋＷとした場合に、近似関数Ｙ＝ａ／Ｘを使用して同様にフィッティングさせると、図中の実線２２に示すように、実測点とフィッティングカーブが大きくずれる。これは、実測点の一部が上記数式１を満足していないことを示す。

【００２７】そこで、スパッタリングパワーを１．１ｋＷとした場合について、放電を開始してから約３秒後の実測点を除いて、近似関数Ｙ＝ａ／（Ｘ－ｂ）を使用してフィッティングさせると、図中の波線２３に示すように、スパッタリングパワーを４．４ｋＷとした場合と同

様に、近似関数と実測値とが一致する。これにより、除去した実測点が上記数式を満足していないことが示される。即ち、スパッタリングパワーを１．１ｋＷとした場合には、放電を開始してから約３秒間においては連続膜が形成されず、島状態の不連続なＴｉ膜が素子上に点在することが示される。なお、点在する不連続膜であっても、隣り合う膜と膜との間隔が数Å乃至数１０Åであれば、数Ｖの電圧でもトンネリング効果により電流が流れるので、シート抵抗として測定できる。そこで、本発明においては、スパッタリング時間によるシート抵抗の実測値が、数式Ｙ＝ａ／Ｘ（ａは定数）で近似される場合に連続した膜が形成されたとみなす。但し、この実測値は厳密に上記数式上にある必要はなく、上記数式から±４０％以内の範囲に実測値があればよいものとする。

【００２８】図３は縦軸にゲート耐圧の不良発生率をとり、異なるスパッタリングパワーでＴｉ膜を成膜した場合の不良発生率を示すグラフ図である。なお、不良発生率は、成膜開始から１秒後までに連続膜が形成される実施例条件（スパッタリングパワー：４．４ｋＷ）でＴｉシリサイド層を形成するためのＴｉ膜を成膜した場合と、成膜開始してから約３秒間において島状態の不連続なＴｉ膜が形成される比較例条件（スパッタリングパワー：１．１ｋＷ）で成膜した場合とにおいて比較した。

【００２９】不良発生率の測定方法について、以下に説明する。先ず、図１（ａ）に示す構造の試験片をテストパターンとして作製した後、その表面上にスパッタリングによるＴｉ膜の形成及び除去を実施して、ゲート電極と基板との間に０乃至１２Ｖの電圧を可変的に印可する。このとき、ゲート酸化膜が絶縁破壊されて大電流が流れる電圧を測定し、この電圧が３Ｖ以下の場合を不良として判定する。そして、測定点数に対する不良数を不良率として計算する。なお、絶縁破壊されていない正常なゲート酸化膜の場合には、その膜厚及び面積にも依存するが、例えば、膜厚が約１００Åであり、面積が約３２mm^2であれば、約１０Ｖの耐圧性を得ることができる。

【００３０】図３に示すように、スパッタリングパワーを４．４ｋＷとしてＴｉ膜を成膜した場合には、この条件は、Ｔｉ膜の成膜開始から１秒後までに連続したＴｉ膜が形成される条件であるので、ゲート酸化膜の耐圧不良率が極めて低く、０．５８％となった。これに対して、スパッタリングパワーを１．１ｋＷとしてＴｉ膜を成膜した場合には、放電を開始してから約３秒間において島状態の不連続膜が形成されているので、不良率が１４．５３％となり、実施例と比較して不良率が約２５倍に増加している。このように、成膜開始から１秒後までに連続膜が形成されるような条件で、スパッタリングによりＴｉ膜を形成すると、ゲート酸化膜の耐圧不良の発生を抑制する効果を得ることができる。

【００３１】なお、図１に示す実施例においては、ＤＣパワーを従来の範囲よりも高くすることにより、Ｔｉ膜の成膜レートを上昇させて、成膜開始から１秒後までに連続膜が形成されるような条件を設定したが、本発明においては、ＤＣパワー以外の条件を変化させてもよい。例えば、スパッタリング時のガス圧力等の他の成膜パラメータを最適化したり、放電用のカソードマグネットを最適化する方法を使用しても、成膜開始から１秒後までに連続した金属膜が形成できる条件であれば、スパッタリングパワーを４．４ｋＷとした場合と同様の効果を得ることができる。

【００３２】また、上記実施例では、Ｔｉ膜の成膜方法としてスパッタリングを使用した場合について示したが、本発明においては、例えば、プラズマＣＶＤ法等を使用して本発明に規定する条件でＴｉ膜を形成しても、同様の効果を得ることができる。更に、上記実施例においては、Ｔｉシリサイド層を形成するためＴｉ膜の成膜時の条件について示したが、本発明においては、例えば、Ｃｏ、Ｎｉ、Ｍｏ、Ｗ及びＴａ等のように、シリコンと反応してシリサイド層を形成する金属膜であれば、同様の効果を得ることができる。

【００３３】

【発明の効果】以上詳述したように、本発明によれば、素子上に形成する金属膜の成膜条件を適切に規定して、金属膜の成膜開始から１秒後までに連続膜が形成されるようにするので、金属膜が帯電することにより発生する絶縁膜の破壊を防止することができ、これにより信頼性が高い半導体装置を高歩留まりで製造することができる。

【図面の簡単な説明】

【図１】（ａ）乃至１（ｄ）は本発明の実施例に係る半導体装置の製造方法を工程順に示す断面図である。

【図２】縦軸にシート抵抗をとり、横軸にスパッタリング時間をとって、スパッタリングパワーを４．４ｋＷとした場合と、スパッタリングパワーを１．１ｋＷとした場合とのシート抵抗とスパッタリング時間の関係を示すグラフ図である。

【図３】縦軸にゲート耐圧の不良発生率をとり、異なるスパッタリングパワーでＴｉ膜を成膜した場合の不良発生率を示すグラフ図である。

【図４】（ａ）は従来の製造方法を使用して素子上に金属膜を形成した場合の金属膜の初期状態を示す断面図であり、図４（ｂ）は本発明に係る製造方法を使用して素子上に金属膜を形成した場合の金属膜の初期状態を示す断面図である。

【図５】（ａ）乃至５（ｄ）はＴｉシリサイド層を利用して動作速度の向上を図った従来の半導体装置の製造方法を工程順に示す断面図である。

【図６】ＤＣマグネトロンによる通常のスパッタリング法を示す模式図である。

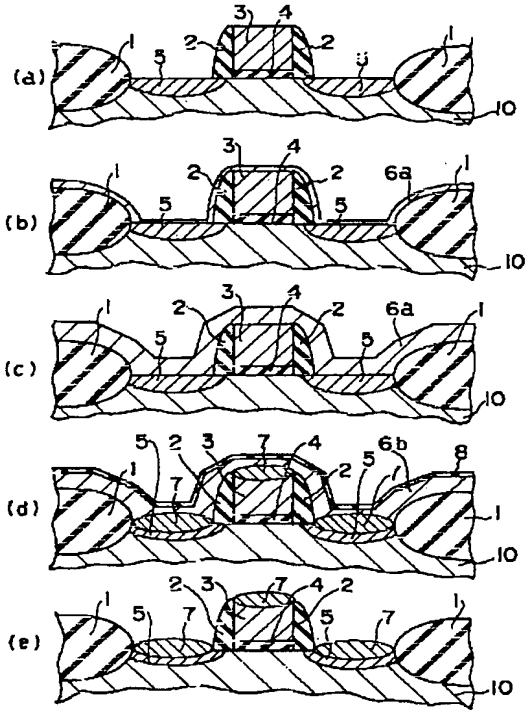
【図７】コリメートスパッタリング法を示す模式図であ

る。

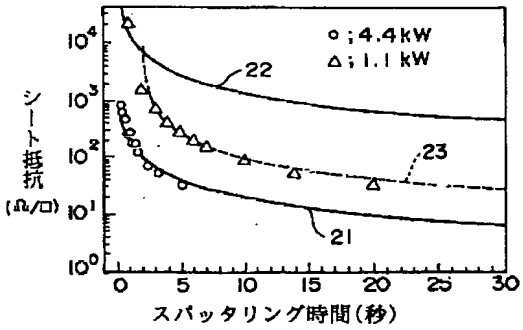
【符号の説明】

1，1-1；素子分離膜
2，12；側壁絶縁膜
3，13；ゲート電極
4，14；ゲート酸化膜
5，15；拡散層
6a，6b，19a，19b，19c；Ti膜
7，17；Tiシリサイド層
8，18；TiN層
10，20；半導体基板
31；ターゲット
32；プラズマ
33；基板
34；ステージ
35；コリメータ
36；カソードマグネット

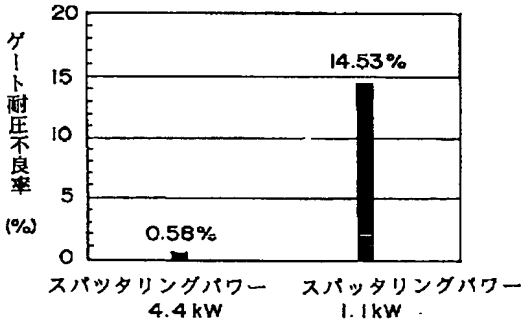
【図1】



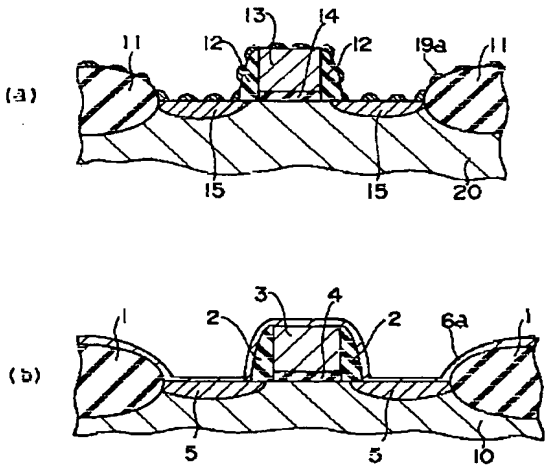
【図2】



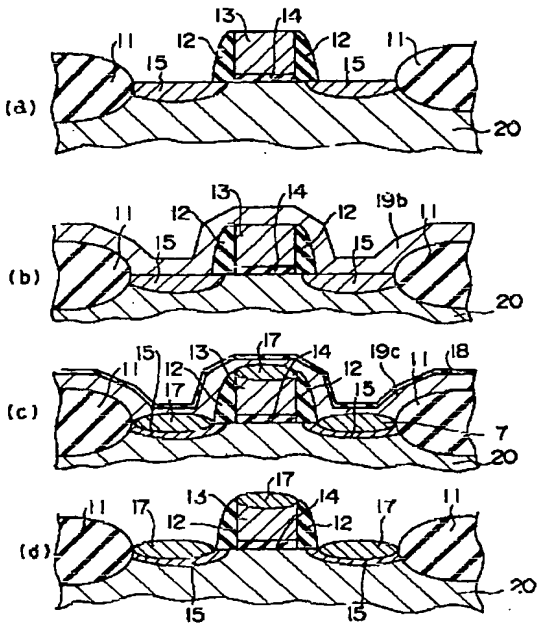
【図3】



【図4】

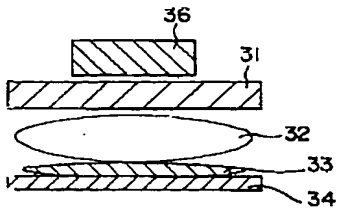


【図５】

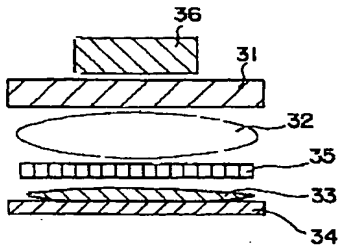


１１；素子分離膜　　１７；Ｔｉシリサイド層
１２；仮想絶縁膜　　１８；ＴｉＮ層
１３；ゲート電極　　１９ｂ，１９ｃ；Ｔｉ膜
１４；ゲート酸化膜　　２０；半導体基板
１５；拡散層

【図６】



【図７】



３１；ターゲット　　３４；ステージ
３２；プラズマ　　３５；コリメータ
３３；基板　　３６；カソードマグネット